REMARKS

Claims 1-6, 8-13 and 15-20 are in the application. Claims 7 and 14 have been cancelled.

By this amendment, claim 1 has been amended to more particularly point out the subject matter of applicant's invention. FIG. 1 and cancelled claim 7 support these changes. Claim 8 has been amended to now depend from claim 1. Claim 9 has been amended to more particularly point out the subject matter of applicant's invention. FIG. 1 supports the change to claim 9. Claim 12 has been amended to more particularly point the subject matter of applicant's invention. FIG. 1, paragraph [0029], and cancelled claim 14 support the changes to claim 12. Claim 18 has been amended to more particularly point out applicant's invention. Cancelled claims 7 and 14 support the changes to claim 18.

Amendment Submitted in Compliance With 37 CFR 1.116(b)(3)

Applicant respectfully submits that this amendment touches the merits of his application, and it is necessary and was not earlier presented because the Examiner has now cited prior art not previously presented or considered. Applicant further believes that this amendment places his application in better form for allowance or consideration on appeal, and respectfully requests its admission.

Response to First 35 U.S.C. §103 Rejection

Claims 1, 4, 5, 7-12, 14-18, and 20 were rejected under 35 U.S.C. §103 as being obvious over Blanchard, USP 4,914,058 (hereafter "Blanchard") in view of Yanagisawa, U.S. Publication 2005/0032280 (hereinafter "Yanagisawa"). This rejection is respectfully traversed in view the amendments made herein and the remarks presented hereinafter. Claims 7 and 14 have been cancelled by this amendment making the rejection of these two claims now moot.

Claim 1 calls for a method of making a semiconductor vertical FET device including the steps of providing a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact. The method also calls for forming a first trench in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface. The method additionally calls for forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface. The method further calls for forming a first source region in the body of semiconductor material extending from the upper surface and spaced apart from the first trench by a portion of the body of semiconductor material. The method still further calls for introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate

region, wherein the doped gate region extends into the body of semiconductor material. Moreover, the method calls for forming a first passivation layer over the doped gate region, and forming a second passivation layer over the first passivation layer thereby filling at least the second trench.

Applicant respectfully submits that the Blanchard and Yanagisawa references fail to make claim 1 obvious for at least the following reasons. Specifically, both references fail to show or suggest a source region spaced apart from the first trench by a portion of the body of semiconductor material. In both references, the source regions abut or terminate against the first trench portion. Further, applicant respectfully submits that this is not a minor difference. As stated in the specification in paragraph [0029], the separation between the source region and doped gate helps, among other things, improve gate blocking characteristics.

Additionally, applicant respectfully submits that the Yanagisawa reference does not show or suggest a doped gate region as is called for in claim 1. Specifically, the Yanagisawa device is a MOSFET device, so the Yanagisawa gate region is the polysilicon region 106, which is separated from the semiconductor layers by a gate oxide 105. In fact, paragraphs [0039]-[0041] in the Yanagisawa reference specifically state that the gate conductors are formed over gate insulators, which are on each inner peripheral surface of the trenches. Yanagisawa further states in paragraph [0057] that "[t]he trench gate electrode 106a functions as a MOS gate." Thus, this is clear evidence that Yanagisawa's gate regions are not in the semiconductor layer as required

by claim 1, but instead they are separated from the semiconductor layers by gate insulator 105.

The P+ region the Examiner refers to as a doped gate region is in error because that region is a floating region 114, and there is absolutely no indication that region 114 is configured to provide gate control as does applicant's doped gate region. Thus, because both references fail to show or suggest introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region extends into the body of semiconductor material, these references fail to make claim 1 obvious.

Moreover, applicant believes that claim 1 is allowable over Blanchard and Yanagisawa because neither reference shows or suggests forming a first passivation layer over the doped gate region, and forming a second passivation layer over the first passivation layer thereby filling at least the second trench. In Blanchard, the second trench has one passivation layer, and it is filled with doped polysilicon. Moreover, Blanchard does not even show or suggest a second passivation layer the first. In Yanagisawa, the single trench has one passivation layer, and is filled with doped polysilicon. Further, Yanagisawa does not suggest a second passivation layer.

Claims 4, 5 and 8 depend from claim 1 and are believed allowable over the cited references for at least the same reasons as claim 1.

Claim 9 depends from the claim 1 and further calls for a second source region formed in the body of semiconductor material spaced apart from the trench by another portion of

the body of semiconductor material. Claim 9 is believed allowable for at least the same reasons as claim 1.

Additionally, applicant respectively submits that claim 9 is allowable over the cited references because neither one shows or suggests a second source region spaced apart from the first trench by another portion of the body of semiconductor material. In Blanchard, the source regions abut the first trench. In fact as shown in FIG. 4b of Blanchard, the first trench is etched directly through the source regions 21a and 21b. In Yanagisawa, the source regions 108 abut the trenches 112, and are not separated by another portion of the semiconductor material.

Claims 10 and 11 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 12 calls for a process for making a compound semiconductor vertical junction FET device comprising the steps of forming a first groove in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first surface of the compound semiconductor layer. The process also calls for forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface. In addition, the process includes doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a doped gate region in the compound semiconductor layer, and forming a first source region of the first conductivity type in the compound semiconductor layer adjacent to the first groove. Additionally, the process includes forming a source contact to the first source region, and filling the second groove and at least a portion of the first groove with a

passivation layer. Further, the process calls for forming a drain contact on a second surface of the compound semiconductor layer.

Applicant respectfully submits that Blanchard and Yanagisawa fail to make claim 12 obvious for at least the following reasons. First, neither Blanchard nor Yanagisawa show or suggest doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a doped gate region in the compound semiconductor layer.

The Office Action admits that Blanchard does not show such a region, and applicant respectfully submits that the Yanagisawa reference does not show or suggest one either. Specifically, the Yanagisawa device is a MOSFET device, not a junction FET device as claim 12 calls for, so the Yanagisawa gate region is the polysilicon region 106, which is separated from the semiconductor layers by a gate oxide 105. In fact, paragraphs [0039]-[0041] in the Yanagisawa reference specifically state that the gate conductors are formed over gate insulators. The gate insulators are on each inner peripheral surface of the trenches and between the gate conductors and the semiconductor layers. Yanagisawa further states in paragraph [0057] that "[t]he trench gate electrode 106a functions as a MOS gate." Thus, this is clear evidence that Yanagisawa's gate regions are not in the semiconductor layer as required by claim 12, but instead they are separated from the compound semiconductor layers by gate insulator 105.

The P+ region the Examiner refers to is a floating region 114, and there is absolutely no indication that region 114 is configured to provide gate control as does applicant's doped gate region. Thus, because both

references fail to show or suggest introducing a dopant of a second conductivity type into at least a portion of the second sidewalls and the second bottom surface to form a doped gate region, wherein the doped gate region extends into the body of semiconductor material, these references fail to make claim 12 obvious.

Additionally, claim 12 has been amended to call for the step of filling the second groove and at least a portion of the first groove with a passivation layer. Applicant further submits that neither reference either singularly or in combination shows or suggests this step. Specifically, Blanchard's second groove is only partially filled with passivation with the balance filled with polysilicon. Thus, claim 12 is believed allowable for the additional reason.

Claims 15-17 depend from claim 12 and are believed allowable for at least the same reasons as claim 12.

Claim 18 calls for a method for forming a compound semiconductor FET device comprising the steps of providing a body of compound semiconductor material including a support wafer of a first conductivity type and a first dopant level and an epitaxial layer formed over the support wafer, wherein the epitaxial layer is of the first conductivity type and has a second dopant level lower than the first dopant level. The method also calls for forming a plurality of spaced apart first doped regions of the first conductivity type in the epitaxial layer, and forming a plurality of first trenches in the epitaxial layer, wherein each first trench is between a pair of first doped regions. Additionally, the method calls for forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench, and doping at least portions of sidewall surfaces and lower surfaces of each

second trench to form a plurality of doped gate regions, wherein the plurality of doped gate regions extend into the body of compound semiconductor material. In addition, the method calls for coupling the plurality of spaced apart first doped regions with a first contact layer, and coupling the plurality of doped gate regions to a gate connecting region formed in the body of compound semiconductor material. Further, the method calls for forming a drain contact on a second surface of the support wafer.

Applicant respectfully submits that Blanchard and Yanagisawa fail to make claim 18 obvious for at least the following reasons. First, neither reference shows or suggests the step of coupling the plurality of doped gate regions to a gate connecting region formed in the body of compound semiconductor material. In fact, both references are completely silent as to how their gate regions are tied together, and there certainly is no suggestion that they tied together as claim in claim 18. Applicant further submits that this is not a minor difference. Specifically, as stated in paragraph [0034] of applicant's specification, applicant's method as claimed allows, among other things, the individual doped gate regions to be placed closer together by providing a contact region. This allows doped gate regions 59 to extend along channels 61, which improves gate blocking capability.

Additionally, claim 18 has been amended to call for the step of filling the second groove and at least a portion of the first groove with a passivation layer. Applicant further submits that neither reference either singularly or in combination shows or suggests this step. Specifically, Blanchard's second groove is only partially filled with

passivation with the balance filled with polysilicon. Thus, claim 18 is believed allowable for the additional reason.

Claim 20 depends from claim 18 and is believed allowable for at least the same reasons as claim 18.

Response to Second 35 U.S.C..§103 Rejections

Claims 2, 3, 6, 13, 19 were rejected under §103(a) as being unpatentable over Blanchard in view of Yanagisawa and further in view of Tews et al. USP 6,335,247 (hereinafter "Tews") and Plumton et al., USP 6,229,197 (hereinafter "Plumton"). This rejection is respectfully traversed in view of the amendments made herein and the remarks presented hereinafter.

Claims 2, 3, and 6 depend from claim 1. Applicant respectfully submits Tew and Plumton do no overcome the shortcomings of Blanchard and Yanagisawa set forth above in response to the rejection of claim 1, and therefore, claims 2, 3, and 6 are believed allowable for at least the same reasons as claim 1.

Claim 13 depends from claim 12. Applicant respectfully submits Tew and Plumton do no overcome the shortcomings of Blanchard and Yanagisawa set forth above in response to the rejection of claim 12, and therefore, claim 13 is believed allowable for at least the same reasons as claim 12.

Claim 19 depends from claim 18. Applicant respectfully submits Tew and Plumton do no overcome the shortcomings of Blanchard and Yanagisawa set forth above in response to the rejection of claim 18, and therefore, claim 19 is believed allowable for at least the same reasons as claim 18.

In view of all of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Peyman Hadizad

ON Semiconductor
Intellectual Property Dept.
P.O. Box 62890; M/D A700
Phoenix, AZ 85082-2890

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Kevin B. Jackson
Attorney for Applicant
Reg. No. 38,502
Tel. (602) 244-4885